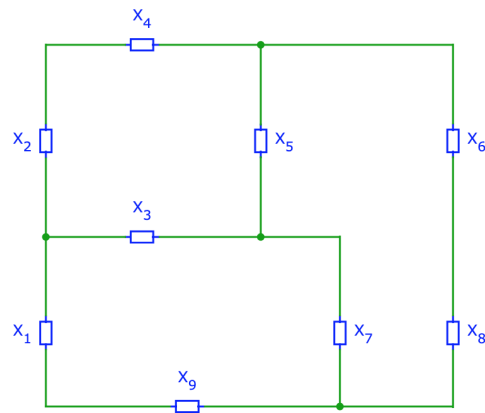

EECS 16A Designing Information Devices and Systems I

Fall 2020 Discussion 6B

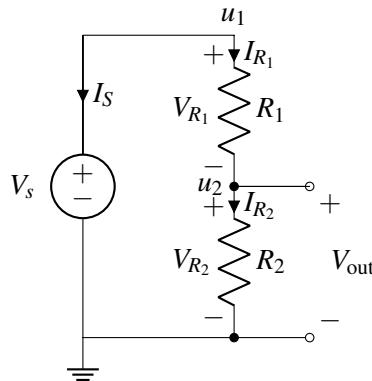
1. Nodes and Branches

In the circuit shown below, label and count all nodes and branches.



2. Voltage Divider

For the circuit below, your goal will be to find the voltage V_{out} in terms of the resistances R_1 , R_2 , and V_s , using NVA (Node Voltage Analysis). The labeling steps (steps 1-4) have already been done for you.

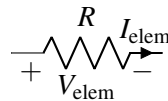


Here is a reminder of the labeling steps followed to get the circuit diagram above:

- **Step 1:** Select a reference (ground) node. Any node can be chosen for this purpose. We will measure all of the voltages in the rest of the circuit relative to this point.
- **Step 2:** Label all nodes with voltage set by voltage sources.
- **Step 3:** Label remaining nodes.
- **Step 4:** Label element voltages and currents, following **Passive Sign Convention** (discussed below).

Passive sign convention

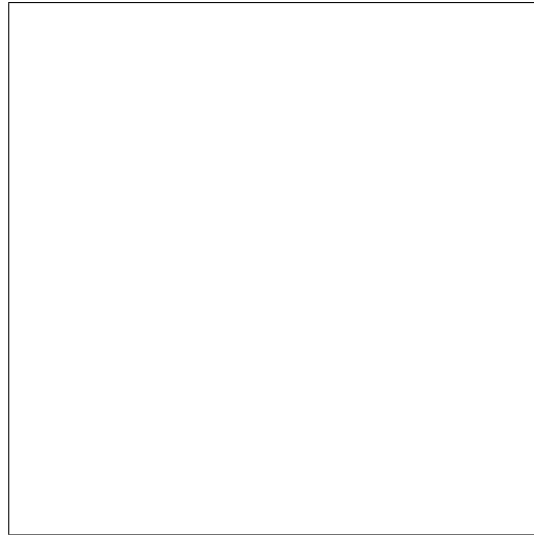
The **passive sign convention** dictates that positive current should *enter* the positive terminal and *exit* the negative terminal of an element. Below is an example for a resistor:



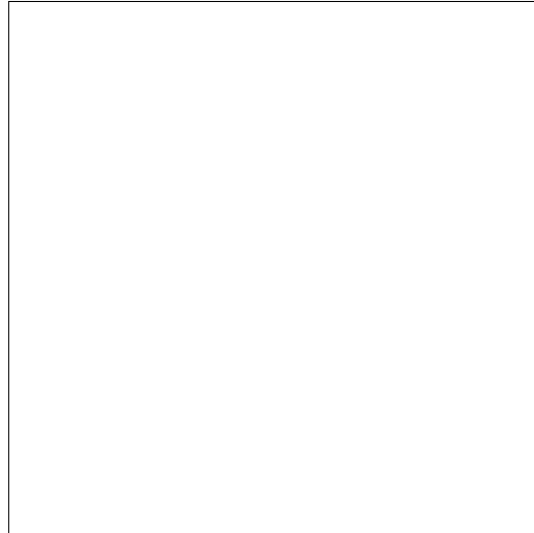
As long as this convention is followed consistently, it does not matter which direction you arbitrarily assigned each element current to; the voltage referencing will work out to determine the correct final sign. When we discuss *power* later in the module, you will see why we call this convention “passive.”

To achieve your goal of *finding* V_{out} , perform the rest of the NVA steps in the boxes below:

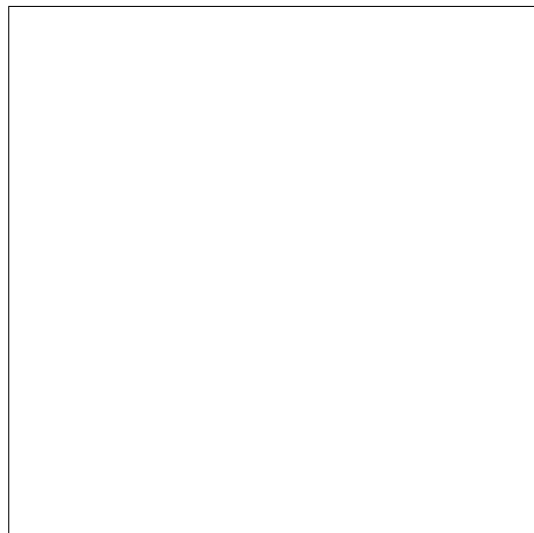
Step 5: Write KCL equations for all nodes with unknown voltages.

A large empty rectangular box intended for the student to write KCL equations for nodes with unknown voltages.

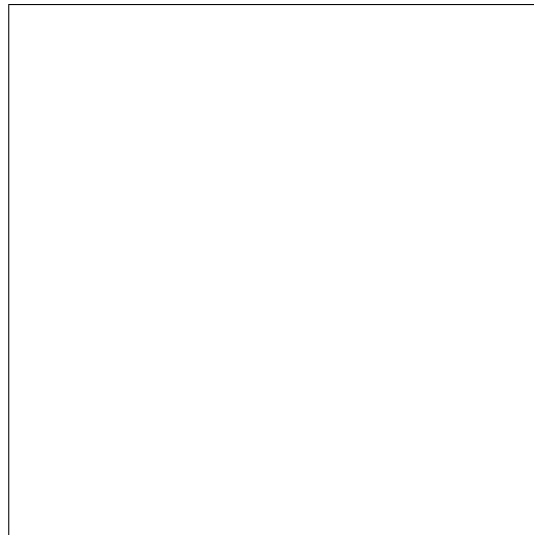
Step 6: Find expressions for all element currents in terms of element voltages and characteristics.

A large empty rectangular box intended for the student to find expressions for all element currents in terms of element voltages and characteristics.

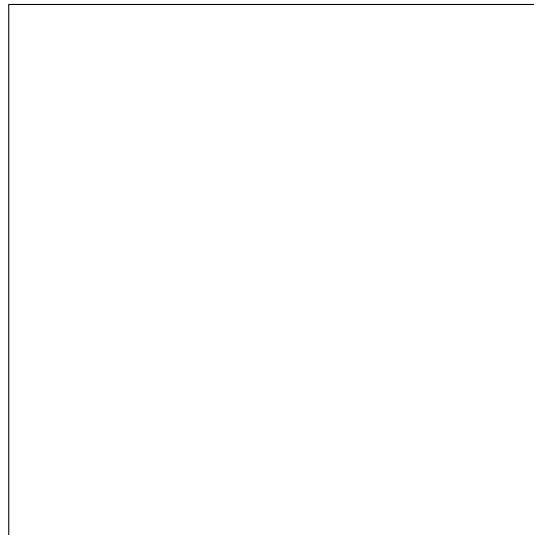
Step 7: Substitute all element voltages with node voltages found in your step 6 equations.

A large empty rectangular box intended for the student to substitute all element voltages with node voltages found in their step 6 equations.

Step 8: Substitute expressions found in step 7 into the KCL equations from step 5.



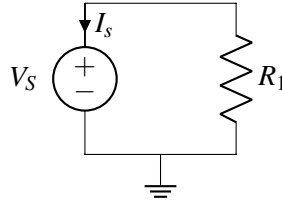
Step 9: Solve for the node voltage values. At this point the analysis procedure is effectively complete - all that's left to do is solve the system of linear equations (by applying Gaussian Elimination, inverting \mathbf{A} , etc.) to find the values for the u 's. Then we can go back to our Step 7 equations and calculate the I 's. Note that in our circuit, $V_{out} = u_2 - 0 = u_2$.



3. Practice: A Simple Circuit

Use KVL and/or KCL to solve the following circuits.

- (a) For this problem assume $V_S = 1V$ and $R_1 = 1k\Omega$. Find the current, I_s flowing through the voltage source.



- (b) For this problem assume $V_S = 1V$, $R_1 = 2k\Omega$, and $R_2 = 2k\Omega$. Find the current, I_s flowing through the voltage source.

