This homework is due November 5, 2021, at 23:59.
Self-grades are due November 8, 2021, at 23:59.

Submission Format
Your homework submission should consist of one file.

- hw10.pdf: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

1. Reading Assignment
No submission is required for this problem, however we ask that you read and understand the notes.
For this homework, please read Note 17A to learn about comparators and op-amps, and Note 17B to learn about charge sharing. You are always encouraged to read beyond this as well.

(a) If the op-amp supply voltages are $V_{DD} = 5\,\text{V}$ and $V_{SS} = 0\,\text{V}$, then what is the minimum/maximum value of $V_{out}$?

(b) What is the purpose of a comparator? How can we use a comparator circuit to detect a touch for a capacitive touchscreen?

Solution:

a) The minimum op-amp output will always be the value of the $V_{SS}$ supply rail, and thus 0V in this case. The maximum op-amp output will always be the value of the $V_{DD}$ supply rail, and thus 5V in this case.

b) A comparator gives a binary output of either a high value or a low value depending on the difference of voltage between its two input terminals. Thus, comparators can be used as indicators or switches. In the case of a touchscreen, a comparator can indicate whether or not a touch occurs. This can be done by hooking up one of the comparator terminals to the equivalent capacitance of the touchscreen, and the other terminal to a reference voltage source. The value of this reference voltage source needs to be between the peak of the voltage over the capacitor with and without touch. Thus, when a touch occurs, the difference between the input terminals will invert in sign, and the comparator will respond.

2. Charge Sharing
Consider the following circuit:
In the first phase, all of the switches labeled \( \phi_1 \) will be closed and all switches labeled \( \phi_2 \) will be open. In the second phase, all switches labeled \( \phi_1 \) are opened and all switches labeled \( \phi_2 \) are closed.

(a) Draw the polarity of the voltage (using + and − signs) across the two capacitors \( C_1 \) and \( C_2 \). (It doesn’t matter which terminal you label + or −; just remember to keep these consistent through phase 1 and 2!)

**Solution:**

One way of marking the polarities is + on the top plate and − on the bottom plate of both \( C_1 \) and \( C_2 \). Let’s call the voltage drop across \( C_1 \) \( V_{C_1} \) and across \( C_2 \) \( V_{C_2} \).

(b) Draw the circuit in the first phase and in the second phase. Keep your polarity from part (a) in mind.

**Solution:**
In phase 1, all the switches marked as $\phi_1$ are closed and switches marked as $\phi_2$ are open. In phase 2, all the switches marked as $\phi_2$ are closed and switches marked as $\phi_1$ are open. Draw both the circuits separately, side by side, with the switches in their respective positions.

(c) Find the voltage across and the charge on $C_1$ and $C_2$ in phase 1. Be sure to keep the polarities of the voltages the same!

**Solution:**

In phase 1,

$$V_{C_{1,1}} = V_{\text{source}} - 0 = V_{\text{source}}$$

and

$$V_{C_{2,1}} = 0 - 0 = 0$$

Next, we find the charge on each capacitor in phase 1:

$$Q_{C_{1,1}} = V_{C_{1,1}}C_1 = CV_{\text{source}}$$

Note that the positive plate has a charge of $+CV_{\text{source}}$, while the negative plate has a charge of $-CV_{\text{source}}$.

$$Q_{C_{2,1}} = V_{C_{2,1}}C_2 = 0$$

(d) Now, in the second phase, find the voltage $V_x$.

**Solution:**

Where is charge conserved? To answer this, look at the top plates of $C_1$ and $C_2$. In phase 2, they are both “floating” because they are not connected to $V_{\text{source}}$ or ground. And in phase 1, they are not connected to each other, but in phase 2, they are connected by the switch. Therefore, in phase 2, the charges on the top plates of $C_1$ and $C_2$ will be shared, or distributed, because they simply cannot go anywhere else. The total charge will remain the same as in phase 1. Let’s find the voltages across $C_1$ and $C_2$ in phase 2 (same polarities as in phase 1!):

$$V_{C_{1,2}} = V_x - V_{\text{source}}$$

and

$$V_{C_{2,2}} = V_x$$

Now, let’s find the charge stored in top plates of $C_1$ and $C_2$:

$$Q_{C_{1,2}} = C_1(V_x - V_{\text{source}}) = C(V_x - V_{\text{source}})$$
and
\[ Q_{c2,2} = C_2 V_x = 9CV_x \]

Next, let’s write the equation for charge conservation:
\[ Q_{c1,1} + Q_{c2,1} = Q_{c1,2} + Q_{c2,2}, \]
giving
\[ CV_{source} + 0 = C(V_x - V_{source}) + 9CV_x, \]
which results in
\[ V_x = \frac{V_{source}}{5}. \]

(e) If the capacitor \( C_2 \) did not exist (i.e. had a capacitance of 0F), what would the voltage \( V_x \) be?

**Solution:**

We could always go back to the equations above, plug in \( C_2 = 0 \), and derive \( V_x = 2V_{source} \). It might be worthwhile to go over what this means for the circuit, though. If \( C_2 = 0 \)F, the capacitor is actually an open circuit. (Why?) So we can pretend, as the question says, that \( C_2 \) does not exist. In phase 1, as before, \( C_1 \) has a voltage drop of \( V_{source} \) across it (from top to bottom) and is charged up to \( CV_{source} \).

Now, in phase 2, the top plate of \( C_1 \) is left dangling (floating). This means that the charge on the top plate of \( C_1 \) is going to be the same just like the charge on the bottom plate. We will therefore get
\[ V_x = V_{source} - (-V_{source}) = 2V_{source} \]

Intuitively, we can think of the capacitor \( C_1 \) as a "temporary battery". In phase 1, \( C_1 \) is charged with a certain \( Q = C_1 V_{source} \). In phase 2, when \( C_2 = 0 \) (i.e. doesn’t exist), the node \( V_x \) is floating and so the charge on \( C_1 \) has nowhere to go. In other words, the charge on \( C_1 \) does not change, so the voltage across \( C_1 \) does not change. This means that there is a voltage increase of \( V_{source} \) from its bottom plate to top plate. Now that the bottom plate is connected to \( V_{source} \), that means its top plate must have a value of \( 2V_{source} \).

If there were no resistive losses in the circuit, this "temporary battery" would set \( V_x = 2V_{source} \) forever. However, any real circuit has some resistances (either by design or due to unintended switch resistances), and these resistances will "drain" the battery and decay the voltage \( V_x \) over time. You will learn more about this transient decay (time constants) in EECS16B.

**Recipe for charge sharing:**

1. Label the voltages across all the capacitors. Choose whichever direction (polarity) you want for each capacitor - this means you can mark any one of the plates with the “+” sign, and then you can mark the other plate with the “-” sign. Just make sure you stay consistent with this polarity across phases.

2. Draw the equivalent circuit during both phases (Phase 1: \( \phi_1 \) closed, \( \phi_2 \) open - Phase 2: \( \phi_1 \) open, \( \phi_2 \) closed). Also, label all node voltages on the circuit for both phases. No need to try and maintain the same names, since certain nodes of the Phase 1 circuit might be merged or split in Phase 2.

3. Identify all “floating” nodes in your circuit during Phase 2. A floating node is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, op-amp inputs or comparator inputs. These will be the nodes where we apply charge sharing.
4. Pick a floating node from the ones you found in Step 3 and identify all capacitor plates connected to that node during Phase 2. Then, calculate the charge on each of these plates during Phase 1. To do so, identify all nodes in your circuit during Phase 1. Label all node voltages, and write the voltages across each capacitor as functions of node voltages (Step 2 should help you with that). Do this according to the polarities you have selected. Then the charge is found as $Q = CV_C$ (where $V_C$ is the voltage across a capacitor).

5. Find the total charge on each of the floating nodes during Phase 2 as a function of node voltages. Use the same process as in Step 4, but this time using the node voltages during Phase 2 to write the voltages across each capacitor. Make sure you kept the polarity same and pay attention to the sign of each plate.

6. Equate the total charge calculated in Phase 1 (Step 4) to the total charge calculated in Phase 2 (Step 5) (charge conservation).

7. Repeat Steps 4-6 for every floating node. This will give you one equation per floating node (i.e. if you have $m$ floating nodes you will have $m$ equations). You can then solve the system of equations to find the node voltages during Phase 2 (unknowns). It should have a unique solution!

As you probably noticed this exercise was architected in a way that basically walked you through this recipe used to approach charge sharing problems.

3. It’s finally raining!

A lettuce farmer in Salinas Valley has grown tired of weather.com’s imprecise rain measurements. Therefore, they decided to take matters into their own hands by building a rain sensor. They placed a square tank outside and attached two metal plates to two opposite sides in an effort to make a capacitor whose capacitance varies with the amount of water inside.

![Tank side view and top view](image)

The width and length of the tank are both $w$ (i.e., the base is square) and the height of the tank is $h_{tot}$.

(a) What is the capacitance between terminals $a$ and $b$ when the tank is full? What about when it is empty?

*Note:* the permittivity of air is $\varepsilon$, and the permittivity of rainwater is $81\varepsilon$.

**Solution:**
Capacitance of parallel plates is governed by the equation:

\[ C = \varepsilon \frac{A}{d}, \]

where \( \varepsilon \) is the permittivity of the dielectric material, \( A \) is the area of the plates, and \( d \) is the distance between the plates. If we apply this to our physical structure, we find that the area of the plates is \( h_{\text{tot}} \cdot w \), and the distance between the plates is \( w \). The only difference here between a full and empty tank is the permittivity of the material between the two plates.

\[ C_{\text{empty}} = \frac{\varepsilon_{\text{air}} h_{\text{tot}} w}{w} = \varepsilon h_{\text{tot}} \]

\[ C_{\text{full}} = \frac{\varepsilon_{\text{H}_2\text{O}} h_{\text{tot}} w}{w} = 81 \varepsilon h_{\text{tot}} \]

(b) Suppose the height of the water in the tank is \( h_{\text{H}_2\text{O}} \). Model the tank as a pair of capacitors in parallel, where one capacitor has a dielectric of air, and one capacitor has a dielectric of water. Find the total capacitance between the two plates using equivalence. Call this capacitance \( C_{\text{tank}} \).

**Solution:**

We can break the total capacitance into two parts. First, let’s calculate the capacitance of the two plates separated by water:

\[ C_{\text{water}} = \frac{\varepsilon_{\text{H}_2\text{O}} h_{\text{H}_2\text{O}} w}{w} = 81 \varepsilon h_{\text{H}_2\text{O}} \]

And now we can calculate the capacitance of the two plates separated by air:

\[ C_{\text{air}} = \frac{\varepsilon_{\text{air}} (h_{\text{tot}} - h_{\text{H}_2\text{O}}) w}{w} = \varepsilon (h_{\text{tot}} - h_{\text{H}_2\text{O}}) \]

These two capacitors appear in parallel, as the result from the layer of water at the bottom of the tank, and the air above the water. Because these two capacitors appear in parallel, we can simply add our two previous results to find the total equivalent capacitance:

\[ C_{\text{tank}} = C_{\text{water}} + C_{\text{air}} = \varepsilon (h_{\text{tot}} + 80 h_{\text{H}_2\text{O}}) \]

(c) After building this capacitor, the farmer consults the internet to assist them with a capacitance-measuring circuit. A fellow internet user recommends the following:

\[ I_s \]

\[ C_{\text{tank}} \]

\[ V_C(t) , V_C(0) = 0 \ V \]

In this circuit, \( C_{\text{tank}} \) is the total tank capacitance that you calculated earlier. \( I_s \) is a known current supplied by a current source.

The suggestion is to measure \( V_C \) for a brief interval of time, and then use the difference to determine \( C_{\text{tank}} \).

Determine \( V_C(t) \), where \( t \) is the number of seconds elapsed since the start of the measurement. You should assume that before any measurements are taken, the voltage across \( C_{\text{tank}} \), i.e. \( V_C \), is initialized to 0 V, i.e. \( V_C(0) = 0 \).
Solution: The element equation for the capacitor is:

\[ I_C = C_{\text{tank}} \frac{dV_C}{dt} \]

We also know from KCL that:

\[ I_C = I_s \]

Thus, we get the following differential equation for \( V_C \):

\[ \frac{dV_C}{dt} = \frac{I_s}{C_{\text{tank}}} \]

We recall that \( I_s \) and \( C_{\text{tank}} \) are constant values and the initial value of \( V_C \) is zero (\( V_C(0) = 0 \)). Applying these facts and integrating the differential equation, we get the following equation for \( V_C \):

\[ V_C(t) = \frac{I_s}{C_{\text{tank}}} t \]

(d) Using the equation you derived for \( V_C(t) \), describe how you can use this circuit to determine \( C_{\text{tank}} \) and \( h_{\text{H}_2\text{O}} \).

Solution: We connect the current source providing \( I_s \) to the capacitor \( C_{\text{tank}} \). At the same time, we can measure \( V_C(t) \). After some time passes, we measure \( V_C(t) \) and plug it into the following equation (assuming, as before, that \( V_C(0) = 0 \)):

\[ C_{\text{tank}} = \frac{I_s}{V_C(t)} t \]

If we know \( C_{\text{tank}} \), we can determine \( h_{\text{H}_2\text{O}} \). Using the equation derived in part (b), we see that

\[ h_{\text{H}_2\text{O}} = \frac{C_{\text{tank}} - h_{\text{tot}} \varepsilon}{80\varepsilon} \]

(e) However, after spending some time thinking about different ways of measuring this capacitance you came up with a better idea. You decided to use the circuit proposed in part (c) along with a comparator, as shown in the figure below. What you are basically interested in, is the time \( T_1 \) needed for \( V_C \) to reach \( V_{\text{ref}} \). In order to measure time you use a timer. When voltage \( V_C \) becomes larger than \( V_{\text{ref}} \), the comparator flips its value and you stop the timer. How would you measure in that case the value of the capacitance?
**Solution:** We connect the current source providing $I_s$ A to the capacitor $C_{tank}$. The expression for $V_C(t)$ can be given by:

$$V_C(t) = \frac{I_s}{C_{tank}}t$$

We are interested at measuring $T_1$ when the $V_c$ reached $V_{ref}$ and the comparator flips. At $T_1$, $V_c$ is equal to $V_{ref}$. Therefore by knowing the reference voltage $V_{ref}$ and measuring with a timer $T_1$, the capacitance can be calculated by:

$$C_{tank} = \frac{I_s T_1}{V_{ref}}$$

If we know $C_{tank}$, we can determine $h_{H_2O}$. Using the equation derived in part (b), we see that

$$h_{H_2O} = \frac{C_{tank} - h_{tot} \varepsilon}{80 \varepsilon}$$

4. **LED Alarm Circuit**

One day, you come back to your dorm to find that your favorite candy has been stolen. Determined to catch the perpetrator red-handed, you decide to put the candy inside a kitchen drawer. Using the following circuit design, you would like to turn on a light-emitting diode (LED) “alarm” if the kitchen drawer is opened.

![LED Alarm Circuit Diagram](image)

Note $R_{photo}$ is a photoresistor, which acts like a typical resistor but changes resistance based on the amount of light it is exposed to. This photoresistor is located inside the kitchen drawer, so we can tell when the drawer is opened or closed.

$V_{LED}$ indicates the voltage across the LED; we will guide you through the IV behavior of this element later in the problem. The LED is located in your room (and connected to a long wire going to the kitchen), so that you can remotely tell when the kitchen drawer has been opened.

(a) What is $V_+$, the voltage at the positive voltage input of the comparator? Your answer should be written in terms of $R_{photo}$ and $R_{fixed}$.

**Solution:** $V_+$ is the output of a voltage divider:

$$V_+ = \frac{R_{fixed}}{R_{fixed} + R_{photo}} \cdot 5 \text{ V}$$
(b) We now want to choose a value for $R_{fixed}$. From the photoresistor’s datasheet, we see the resistance in “light” conditions (i.e. drawer open) is 1kΩ. In “dark” conditions (i.e. drawer closed), the resistance is 10kΩ.

To ensure the comparator detects the light condition with more tolerance, we decide to design $R_{fixed}$ so that $V_+$ is 3 V under the “light” condition. Solve for the value of $R_{fixed}$ to meet this specification.

Solution: We start from the voltage divider equation we derived in the previous part:

$$V_+ = \frac{R_{fixed}}{R_{fixed}+R_{photo}} \cdot 5V$$

Now we plug in the known values, $V_+ = 3V$ and $R_{photo} = 1k\Omega$.

$$3V = \frac{R_{fixed}}{R_{fixed}+1000\Omega} \cdot 5V$$

Solving this equation, we get $R_{fixed} = 1.5k\Omega$.

(c) Write down $V_{out}$ with any conditions in terms of $V_+$. For simplicity, consider the case when $V_+ \neq V_-$ and assume the comparator is ideal.

Solution: Since the comparator is ideal, we know that $V_{out}$ will be the voltage at either the positive rail (5 V) or at the negative rail (0 V) when $V_+ \neq V_-$. Which voltage depends on if $V_+$ is greater than $V_-$ or not. Since $V_-$ is 2.5 V, we get the following piecewise equation for $V_{out}$:

$$V_{out} = \begin{cases} 5V, & V_+ > 2.5V \\ 0V, & V_+ < 2.5V \end{cases}$$

(d) Using your answers to the previous parts, write down $V_{out}$ with the conditions on its output in terms of $R_{photo}$. You can substitute the value of $R_{fixed}$ you found in part (b). As before, you can assume that $V_+ \neq V_-$ and the comparator is ideal.

Solution: We substitute the equations for $V_+$ into the equation for $V_{out}$:

$$V_{out} = \begin{cases} 5V, & R_{photo} < 1.5k\Omega \\ 0V, & R_{photo} > 1.5k\Omega \end{cases}$$

Plugging in $R_{fixed} = 1.5k\Omega$ from part (b), we can get the following in terms of $R_{photo}$:

$$V_{out} = \begin{cases} 5V, & R_{photo} < 1.5k\Omega \\ 0V, & R_{photo} > 1.5k\Omega \end{cases}$$

(e) From the design steps in the previous parts, we have designed a circuit that outputs non-zero voltage when the photoresistor is exposed to light (i.e. kitchen drawer open). We now want to design the LED portion of the circuit, so we get a visual alarm when the drawer is open.

From the LED’s datasheet, the forward voltage, $V_F$ is 3 V. Essentially, if $V_{LED}$ is less than this voltage, the LED won’t light up and $I_{LED}$ will be 0 A.

Here is an idealized IV curve of this LED. The LED behaves in one of the following two modes:
i. If the voltage across the LED is less than \( V_F = 3 \text{V} \) or if \( I_{\text{LED}} < 0 \text{A} \), then the LED acts like an open circuit.

ii. If the voltage across the LED is \( V_F = 3 \text{V} \), then the LED acts like a voltage source, except that it only allows positive current flow (i.e. only in the direction of current marked on the circuit diagram).

To avoid exceeding the power rating of the LED (and having it burn out), the recommended value for \( I_{\text{LED}} \) is 20mA.

Find the value of the current-limiting resistor, \( R_{\text{lim}} \), such that when the photoresistor is in the “light” condition, \( I_{\text{LED}} = 20 \text{mA} \).

**Solution:** When the photoresistor is in the “light” condition, \( R_{\text{photo}} = 1 \text{k}\Omega \), and based on our analysis in the previous part, \( V_{\text{out}} = 5 \text{V} \). This implies that \( V_{\text{LED}} = V_F \) and the LED acts like a power supply with positive current flow when in the “light” condition.

Using Ohm’s Law and noting that the same current passes through \( R_{\text{lim}} \) and the LED itself,

\[
V_{\text{out}} - V_F = I_{\text{LED}} R_{\text{lim}}
\]

Rearranging and plugging in values when in the “light” condition:

\[
R_{\text{lim}} = \frac{V_{\text{out}} - V_F}{I_{\text{LED}}}
\]

\[
R_{\text{lim}} = \frac{5 - 3 \text{ V}}{0.02 \text{ A}}
\]

\[
R_{\text{lim}} = 100 \text{\Omega}
\]

Note that when \( V_{\text{out}} < 3 \text{V} \), the LED will not light up and \( I_{\text{LED}} \) will be 0mA. Thus by our design of the voltage divider, we were able to ensure the LED lights up only if the drawer is opened.

5. **Op-Amp in Negative Feedback**

In this question, we analyze op-amp circuits that have finite op-amp gain \( A \). We replace the op-amp with its circuit model with parameterized gain and observe the gain’s effect on terminal and output voltages as the gain approaches infinity. Figure 1 shows the equivalent model of the op-amp. **Note here that** \( V_{SS} = -V_{DD} \).
For parts (a) - (e) only, assume that the op-amp is ideal (i.e., \( A \to \infty \)). We will consider the case of finite gain \( A \) in parts (f) - (h).

(a) Consider the circuit shown in Figure 2, and again \( V_{SS} = -V_{DD} \). What is \( u_+ - u_- \)?

**Solution:** For ideal op-amp circuits in negative feedback, the voltage at the two terminals must be equal, so \( u_+ - u_- = 0 \).

(b) Find \( v_x \) as a function of \( v_{out} \).

**Solution:** We see that \( v_x \) is the middle node of a voltage divider, so \( v_x = v_{out} \frac{R_1}{R_1 + R_2} \).

(c) What is \( I_{R_2} \), i.e. the current flowing through \( R_2 \) as a function of \( v_s \)? Hint: Find the current through \( R_1 \) first.

**Solution:** We know from part (a) that \( v_x = v_s \). The current flowing through \( R_1 \) is \( I_{R_1} = \frac{v_s}{R_1} \). This current also flows through \( R_2 \).

(d) Find \( v_{out} \) as a function of \( v_s \).

**Solution:** Using the answer from the previous part, \( v_{out} = v_s + R_2 I_{R_1} = v_s + R_2 \frac{v_s}{R_1} = v_s \left( 1 + \frac{R_2}{R_1} \right) \).

(e) What is the current \( i_L \) through the load resistor \( R \)? Give your answer in terms of \( v_{out} \).

**Solution:** The current \( i_L \) through the load is \( \frac{v_{out}}{R} \).

(f) We will now examine what happens when \( A \) is not infinite. To understand what happens in this case, first draw an equivalent circuit for Figure 2, by replacing the ideal op-amp in the non-inverting amplifier in Figure 2 with the op-amp model shown in Figure 1.

Now, using this setup, calculate \( v_{out} \) and \( v_x \) in terms of \( A, v_s, R_1, R_2 \) and \( R \). Is the magnitude of \( v_x \) larger or smaller than the magnitude of \( v_s \)? Do these values depend on \( R \)? Hint: Note that the first golden rule still applies, i.e. the currents through the input terminals are zero.

**Solution:**
This is the equivalent circuit of the op-amp:
Since $v_{out}$ is connected to the output of the op-amp, which is a voltage source, we can determine $v_{out}$:

$$v_{out} = A(u_+ - u_-)$$

$$= A(v_s - v_x)$$

Since there is no current flowing into the op-amp input terminals from nodes $u_+$ and $u_-$, $R_1$ and $R_2$
form a voltage divider and $v_x = v_{out} \left( \frac{R_1}{R_1 + R_2} \right)$. Thus, substituting and solving for $v_{out}$:

$$v_{out} = A \left( v_x - v_{out} \frac{R_1}{R_1 + R_2} \right)$$

$$v_{out} = v_s \left( \frac{1}{R_1} \frac{1}{R_1 + R_2} + \frac{1}{A} \right)$$

Knowing $v_{out}$, we can find $v_x$:

$$v_x = v_s \left( 1 + \frac{R_1}{R_1 + R_2} \right)$$

Notice that $v_x$ is slightly smaller than $v_s$, meaning that in equilibrium in the non-ideal case, $v_+ \neq v_-$ are not equal. $v_{out}$ and $v_x$ do not depend on $R$, which means that we can treat $v_{out}$ as a constant voltage source that supplies a constant voltage independent of the load $R$.

(g) Using your solution to the previous part, calculate the limits of $v_{out}$ and $v_x$ as $A \rightarrow \infty$. You should get the same answer as in part (d) for $v_{out}$.

**Solution:**

As $A \rightarrow \infty$, the fraction $\frac{1}{A} \rightarrow 0$, so

$$v_{out} = v_s \left( \frac{1}{R_1} \frac{1}{R_1 + R_2} + \frac{1}{A} \right)$$

converges to

$$v_s \left( \frac{1}{R_1} \frac{1}{R_1 + R_2} + 0 \right) = v_s \left( \frac{R_1 + R_2}{R_1} \right),$$

Therefore, the limits as $A \rightarrow \infty$ are:

$$v_{out} \rightarrow v_s \left( \frac{R_1 + R_2}{R_1} \right)$$

$$v_x \rightarrow v_s$$

If we observe the op-amp is in negative feedback, we can apply the fact that $u_+ = u_-$. We get $v_x = v_s$. Then the current $i$ flowing through $R_1$ to ground is $\frac{v_s}{R_1}$. By KCL, this same current flows through $R_2$ since no current flows into the negative input terminal of the op-amp ($u_-$). Thus, the voltage drop across $R_2$ is $v_{out} - v_x = i \cdot R_2 = v_s \left( \frac{R_2}{R_1} \right)$. Therefore, $v_{out} = v_s + v_s \left( \frac{R_2}{R_1} \right) = v_s \left( \frac{R_1 + R_2}{R_1} \right)$. The answers are the same if you take the limit as $A \rightarrow \infty$.

(h) **[OPTIONAL, CHALLENGE]** Now you want to make a non-inverting amplifier circuit whose gain is nominally $G_{nom} = \frac{v_{out}}{v_s} = 1 + \frac{R_2}{R_1} = 4$. However, $G_{nom}$ can only be achieved only if the op-amp is ideal, i.e., if its internal gain $A \rightarrow \infty$. But, as with most considerations in the physical world, we must account for nonidealities! In reality, because you will be working with an op-amp with finite gain $A$, your designed circuit gain may come close to but will never quite reach $G_{nom}$ as a result of the real op-amp’s finite internal gain $A$.

Suppose you would like your real op-amp circuit to have a maximum error of 1% (i.e., a minimum circuit gain of 3.96, i.e., $\frac{v_{out}}{v_s} \geq 3.96$). Remember that only if your op-amp were ideal, you would have a nominal circuit gain of $G_{nom} = \frac{v_{out}}{v_s} = 1 + \frac{R_2}{R_1} = 4$.

What is the minimum required value of $A$, called $A_{min}$, to achieve that specification? **Hint:** Use your expression of $v_{out}$ in part (f) to find an expression for $G_{min} = \frac{v_{out}}{v_s}$ when $A \neq \infty$. 

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Solution: From the previous part, \( v_{\text{out}} = v_s \left( \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \right) \). After algebraic manipulations, we get

\[
v_{\text{out}} = v_s \left( \frac{A(R_1 + R_2)}{R_1 + R_2 + AR_1} \right)
\]

We are interested in the op-amp’s minimum gain \( A_{\text{min}} \), which gives us the circuit’s corresponding minimum gain \( G_{\text{min}} \).

We define the minimum (actual - i.e. corresponding to a non-infinite \( A = A_{\text{min}} \)) gain as: \( G_{\text{min}} = \frac{v_{\text{out}}}{v_s} \).

We also define the nominal (ideal - i.e. corresponding to an infinite \( A \)) gain as: \( G_{\text{nom}} = 1 + \frac{R_2}{R_1} \).

Rewriting \( A_{\text{min}} \) in terms of \( G_{\text{nom}} \) and \( G_{\text{min}} \) gives:

\[
A_{\text{min}} = \frac{G_{\text{min}} G_{\text{nom}}}{G_{\text{nom}} - G_{\text{min}}}
\]

\[
= 396
\]

Notice that the op-amp’s minimum gain is independent of the resistor values. In general, if we wanted an error of less than \( \varepsilon \), then the following will approximately hold: \( \frac{A_{\text{min}}}{G_{\text{nom}}} > \frac{1}{\varepsilon} \).

6. Homework Process and Study Group

Who did you work with on this homework? List names and student ID’s. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

Solution:

I first worked by myself for 2 hours, but got stuck on problem 5. Then I met with my study group.

XYZ played the role of facilitator ... etc. We were still stuck on problem 5 so we went to office hours to talk about the problem.

Then I went to homework party for a few hours, where I finished the homework.